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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,707	02/13/2004	Ryohei Nishimiya	1075.1245	5698

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EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,707	NISHIMIYA, RYOHEI	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER 4/19/2006
GROUP 2100
AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/13/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 1-5 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4 and 8 of copending Application No. 11/317011. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-4 and 8 of the reference copending application (11/317011) reiterate almost all the functions and characteristics of the claims 1-5 of the instant application (10/777707).

The difference between the two is that the reference copending application appears to be directed towards a plurality of device units (claims 1-4) and the device

unit is installable to a bus unit (claim 8) while the instant application appears to be directed towards one of the device units among a plurality of device units (claims 1-4) and the device unit connectable to a printed circuit board (claim 5) respectively.

It would have been obvious to one skilled in the art to implement the same configuration that is applied towards one device unit to a plurality of device units, wherein said one device unit is one of the device units among said plurality of device units; and it is well known to one skilled in the art to implement the device unit to be installable on the bus unit, in order for the device unit to be connected to the bus of a printed circuit board, such as the mother board, in the computer system.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. As per claims 1 and 4, applicant recited the limitation "a plurality of device units" at the beginning of the independent claims 1 and 4, but later on recited the limitation "the device unit," "said connected device unit," "said connected device unit," "device unit

connected on said data bus" and "said device unit." It appears unclear how the numerous recitations of the "device unit" relate to the "plurality of device units", if the "device unit" is one of the device unit among the "plurality of device units" or the "device unit" is a different device unit. Examiner will assume that the various recitations of the "device unit" are one of the device units among the "plurality of device units"

4. As per claims 2-3, there are similar recitations of the limitation the "device unit," therefore causing similar unclarity as stated above. The examiner reiterates his arguments and assumption as stated above in claims 1 and 4.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Osaka et al. (US Patent 5,787,261).

6. As per claim 1, Osaka teaches a design method for a bus system equipped with

a plurality of device units (Fig. 1; Fig. 10, ref. 141, 142 and col. 16, ll. 36-63),

a data bus on which one of said plurality of device units are connectible (Fig. 10, ref. 201, 202, 211, 212 and Bus Lines of Fig. 1);

a timing-signal supply source for supplying a timing signal to one of said plurality of device units through a timing-signal bus (clock line transmitting a clock signal,

wherein the clock signal is provided by the back panel 5 of Fig. 1 and col. 12, l. 45 to col. 13, l. 7),

a bus switch for connecting and disconnecting a signal between one of said plurality of device units and said data bus (Fig. 1, ref 11); and

a bus-switch control part for controlling the connecting and disconnecting operations of said bus switch (Fig. 1 ref. 14);

said design method comprising:

a noise propagation computation step of computing, based on a cycle of said timing signal (clock signal from the back panel; col. 12, l. 61 to col. 13, l. 8), a signal propagation delay in one of said plurality of device units (propagation delay of the switch control signal; col. 14, ll. 4-38), signal propagation delays in said timing-signal bus (clock skew; col. 14, ll. 4-38) and said data bus (inherent signal skew similar to the clock skew would be present for the data bus), and a setup time in one of said plurality of device units (the amount of time for the functional circuit board to stabilize after the functional circuit board is connected and powered; col. 6, l. 65 to col. 7, l. 12) or device connected on said data bus, timing at which, when one of said plurality of device units is connected on said data bus being active, noise propagates (propagation of glitch noise; col. 8, ll. 22-38 and col. 8, l. 60 to col. 9, l. 7) to the remaining device units other than said connected one of said plurality of device units (col. 6, l. 65 to col. 9, l. 7 and col. 12, l. 45 to col. 14, l. 38); and

a connection timing computation step of computing, based on said timing computed in said noise propagation computation step, connection timing at which one

of said plurality of device units is connected on said data bus (col. 14, ll. 4-38), wherein the connection time is the delay DELTAt amount of time and then one of said plurality of device units is connected to the data bus (col. 6, l. 65 to col. 9, l. 7 and col. 12, l. 45 to col. 14, l. 38).

7. As per claim 2, Osaka teaches the design method for a bus system further comprising wherein said connection timing computation step said connection timing is computed by computing a delay time "b" (Δt 50 of Fig. 8) needed for said bus switch to connect one of said plurality of device units on said data bus after one of said plurality of device units is connected on said timing-signal bus (col. 13, l. 8 to col. 14, l. 38).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osaka et al. (US Patent 5,787,261).

Osaka teaches design method for a bus system, comprising:

a plurality of device units connectible to a printed circuit board (Fig. 1; Fig. 10, ref. 141, 142 and col. 16, ll. 36-63), wherein the back panel to which the plurality of

device units is connectible to is couple to the printed circuit board (such as the motherboard);

a data bus on which one of said plurality of device units are connectible (Fig. 10, ref. 201, 202, 211, 212 and Bus Lines of Fig. 1);

a timing-signal supply source for supplying a timing signal to one of said plurality of device units through a timing-signal bus (clock line transmitting a clock signal, wherein the clock signal is provided by the back panel 5 of Fig. 1 and col. 12, l. 61 to col. 13, l. 7),

a bus switch for connecting and disconnecting a signal between one of said plurality of device units and said data bus (Fig. 1, ref 11); and

a bus-switch control part for controlling the connecting and disconnecting operations of said bus switch (Fig. 1 ref. 14);

wherein said bus-switch control part controls said bus switch so that one of said plurality of device units is connected on said data bus after a delay time "b" (Δt 50 of Fig. 8) of said bus switch from connection of one of said plurality of device units with said timing-signal bus (col. 13, l. 8 to col. 14, l. 38);

generating the glitch noise after the bus-switch is shift from off to on or on to off and the propagation of said glitch noise resulting in the potential malfunction causing the apparatus connected to the bus lines to function incorrectly (col. 8, l. 22 to col. 9, l. 7), wherein the glitch noise would comprise a pulse width (time) "e" and a propagation delay time "f";

setup time "S" in said bus system (col. 6, l. 65 to col. 7, l. 5), wherein setup time is the amount of time require for the functional circuit board to become stabilized after connecting to the bus line and power supplied,

the generation and distribution of a clock signal within the system, comprising the skew of the clock signal from the source to the associated functional blocks (col. 12, l. 61 to col. 13, l. 7 and col. 14, ll. 4-38);

and wherein, based on cycle "T" of said timing signal (T_{clk}) (col. 14, ll. 4-38),

skew "a" from said timing-signal supply source to said bus switch control part (clock skew of the system) (col. 14, ll. 4-38),

the delay time "b" of said bus switch (Δt or DELTAt) (col. 14, ll. 4-38),

signal propagation delay time "c" between said bus switch control part and said bus switch (propagation delay time of the switch control signal traveling to the switch) (col. 14, ll. 4-38),

operating delay time "d" of said bus switch (switch time T_{pzh}) (col. 14, ll. 4-38),

the delay time "b" of said bus switch is computed as such:

$T > b + (a + c + d)$ (wherein the sum of the value of DELTAt, switching time T_{pzh} of the switch element, propagation delay of the switch signaling and a clock skew of the system is smaller than the bus-clock cycle time T_{clk} ;col. 14, ll. 4-38);

therefore $b < T - (a + c + d)$; and

the resulting time margin is $M = T - (a + c + d) - b = T - (a + b + c + d) - b > 0$, wherein M is 0 or greater.

Osaka teaches the plurality of variables comprising the pulse width (time) "e," the propagation delay time "f," the skew "g" and the setup time "S," (as stated above) but does not expressly teach that the computation of the value M utilizing the above plurality of variables, resulting in the computation of $M = (T + g) - (a + b + c + d + e + f) - S$.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include the plurality of parameters comprising the pulse width (time) "e," the propagation delay time "f," the skew "g" and the setup time "S," into the determination of M, therefore further optimize the time margin M, consisting with the analysis set forth in MPEP 2144.05 under Optimization of Ranges. The resulting equation of time margin would then be

$T > b + (a + c + d) + (e + f) - g + S;$

$b < T - (b + (a + c + d) + (e + f) - g + S) = (T + g) - (a + c + d + e + f) - S;$

$0 < (T + g) - (a + c + d + e + f) - S - b = (T + g) - (a + b + c + d + e + f) - S = M;$

therefore $M = (T + g) - (a + b + c + d + e + f) - S > 0;$

wherein by including the parameters of "e" and "f," the computer system can ensure that glitch noise will never cause malfunction resulting in the apparatus to function incorrectly;

wherein by including the parameter "g", the propagation delay of the clock signal to the rest the apparatus other than current connected functional block (Fig. 1, ref. 3), the time margin M can be increased, therefore loosing the timing requirement for "b"; and

wherein it would be obvious to include the setup time "S" as it is required every time for the functional circuit board to stabilize after connecting to the data bus and powering up before shifting the bus switch from off to on, connecting the functional circuit board to the bus lines, and causing the glitch noise.

Therefore, it would have been obvious to one skilled in the art to include the plurality of parameters comprising the pulse width (time) "e," the propagation delay time "f," the skew "g" and the setup time "S," into the determination of M for the benefit of higher signal integrity for a hot plugging system and method.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.K.L.
04/17/2006

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